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EUROPEAN NUCLEAR SCIENCE AND APPLICATION RESEARCH 2

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D15.10 – REPORT ON CHIP DESIGN

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Disclaimer

This deliverable has been prepared by Work Package 15 (TecHIBA - Technologies for High Intensity Beams and Applications) of the Project in accordance with the Consortium Agreement and the Grant Agreement n°654002. It solely reflects the opinion of the parties to such agreements on a collective basis in the context of the Project and to the extent foreseen in such agreements.

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LIST OF ACRONYMS AND ABBREVIATIONS

GET	General Electronics for Time projection chambers
GES	Generic Electronics System
MoU	Memorandum of understanding
ANR	Agence Nationale de la Recherche
GES-FPCSA CSA	Floating Point Charge Sensitive Amplifier Charge Sensitive Amplifier
ASIC	Application-specific integrated circuit
fpga	field-programmable gate array
SoC	System on Chip

EXECUTIVE SUMMARY

The GES (Generic Electronics System) project represents an important perspective for new generation detectors required by high-resolution experiments with stable and radioactive beams. The need for high segmentation and wide dynamic range in ASIC technologies concerns now also the read-out of solid-state detectors that will be largely employed in experiments with high-intensity stable beams. In this respect, this first deliverable of the project, consisting of providing a report with all the chip specifications that meet a wide community of researchers and engineers, represents an important contribution to the TecHIBA project within the present ENSAR2 programme. The team of researchers and engineers engaged in GES have defined in their report the full specifications of a Floating Point Charge Sensitive Amplifier (FPCSA) that can be used as a high dynamic range pre-amplifier. This chip can be coupled to the already existing GET system, previously developed by the same team in collaboration with other EU and non-EU institutions. The overall work of the team will also consists of developing firmware for the chip that meet the generic requirements characterising the GES project. The following step will consist of building a prototype chip according to the present deliverable report and it will be tested against the simulated features and performances as they are also presented in the following sections of this report.
The report consists of an overall description of the project with details described in three Appendixes. In particular, Appendix III describes all the technical specifications and expected performances for the designed chip. The achievement of the deliverable can be considered successful.

INTRODUCTION

The project **G**eneric **E**lectronics **S**ystem, **GES** had its roots in a previous programme called **GET**. **GET** stands for **G**eneral **E**lectronics for **T**ime projection chambers. **GET** (Ref. 1) was financed by the French, ANR and the US, Department of Energy with a total budget of approximately 700 k€. The prototype system was reproduced industrially. **GET** is today deployed in 24 instruments worldwide covering Japan, China, Korea, Singapore, France, US, Italy, Spain, Poland, Romania and Belgium. **GES** was originally submitted to be analogous to the **GET** development. However, funding restrictions did not allow this. Thus, **GES** has been undersized, particularly in the manpower and the objectives have to be limited in number.

REPORT ON PROGRESS

In the period since allocation of the **GES** budget the following tasks have been undertaken and some of them completed.

A. The **GES** programme as financed by **ENSAR2** had to be reviewed and restructured to achieve lasting yet limited impact on the Nuclear Physics community. So we searched and found European partners that could share the engineering time without funding, in the domain of Firmware and Hardware development. The base context of this collaboration is to initiate and evolve a full *generic* approach. Additional funds are in the process of being applied for. The labs implicated are given in Appendix I.

B. Applying for additional funding for specific tasks.

C. A **MoU** was agreed on and posted for signature. The reason for this is because as for **GET**, the outcome could lead to IP issues. The document is attached in **Appendix I.**

D. A document detailing project content and plan was agreed on. Tasks were attributed to the labs implicated. The document is attached in **Appendix II**.

E. Explicit to the announced deliverable is the definition of the specifications to be achieved in the building of the **ASIC** development called **GES-FPCSA** (**F**loating Point **C**harge **S**ensitive **A**mplifier). The **GES-FPCSA** chip will be extra high dynamic range microelectronics pre-amplifier. It will couple with the GET system. Namely **GES-FPCSA** will be, technically speaking, the very front end of **GET**. In **Appendix III**, the studied specifications that will be undertaken are defined. The following building of the circuit will yield a prototype chip that will be tested against the performances extracted from the simulations.

F. Due to lack of engineering time, the firmware originally built for GET was somewhat specific rendering it rather laborious and hence engineering burdened to modify it for new hardware today available on the market, in particular **fpga** (**f**ield-**p**rogrammable **g**ate **a**rray) circuits. A modular firmware re-build has been framed and underway. Codes running on *Zynq-7000 series* **SoC** (**S**ystem **o**n **C**hip) are being tested presently.

GET with its integration **GES-FPCSA** is a requirement to cover the extra-large dynamic ranges sought in programmes where TPCs are being deployed as active targets. To abide by the designation "generic", **GES-FPCSA** will have the capacity to be reconfigured software wise to treat mores specifically solid-state and photo detectors.

CONCLUSION

The **GES** project while having highly limited resources has by now reached the foreseen objective to establish a four-lab collaboration to develop a study and build a system on a strong generic platform. The deliverable to set the specifications of the ASIC **GES-FPCSA** has been achieved. Furthermore, the tasks definition have been set and undergoing.

Ref 1. E. Pollacco et al.: Physics Procedia 37, 1799 (2012)

Appendix 1: Memorandum of Understanding

THE GES PROJECT

The GES project stands for "Generic Electronics System". It is aimed at developing a chain of generic electronics, comprising hardware, firmware and software modules to be assembled for the purpose of data acquisition on particle detectors. The modules include ASIC chips, electronics boards, and firmware or software components.

The range of applications of the GES modules typically covers nuclear physics experiments, but can naturally extend beyond these to reach other domains such as particle physics, medical imaging and treatments, astrophysics, etc. Many aspects of the GES project can be considered as a follow-up or a spin-off of the GET project (General Electronics for Time Projection Chambers) as they might partly rely on GET hardware, firmware and software designs.

The GES project includes a number of modules to be specified and developed in a collaborative fashion between the different Partners. However, every module (whether hardware, firmware or software), is associated with a task for which a single Partner will be mainly responsible, in accordance with their own scientific and strategic agendas. The development of a module includes design, implementation, test and documentation. *The description of the modules and associated tasks is given in the document entitled "GES Programme ENSAR2 Related Work Packages"* (annexed document).

PURPOSE OF THIS MOU

The purpose of this document is to formalise the partnership between all parties involved in the design, implementation, test and documentation of GES hardware, firmware and software modules. The partnership includes engineering time, schedule and available budget and expertise. The parties are partner institutions collectively referred to as the *GES Partners*.

This MoU covers all activities relevant to the partnership, including:

- ownership and commercial use of all intellectual property (IP) produced within the GES project;
- scientific and technical publications relating to the project itself;
- publications and results pertaining to projects and applications using GES modules.

PARTIES OF THIS MEMORANDUM OF UNDERSTANDING

This Memorandum of Understanding (hereinafter referred to as *MoU*) is established between the following parties, collectively referred to as the *GES Partners*:

Commissariat à l'énergie atomique et aux énergies alternatives, a French state-owned research entity with a scientific, technical or industrial activity duly organised under the laws of France and having its registered office located at Bâtiment Le Ponant D – 25 rue Leblanc, 75015 Paris, France – and declared at the Paris Register of Commerce and Trade (***Registre du Commerce et des Sociétés de Paris***) under registration number R.C.S PARIS B 775 685 019, represented by Mr. Vincent BERGER acting as head of the ***Direction de la recherche***

fondamentale (DRF) and duly authorised for the purpose hereof, acting in its own name and in the name and on behalf of the ***Institut de recherche sur les lois fondamentales de l'univers*** (Irfu) in DRF, hereinafter referred to as *CEA IRFU*;

L'Institut National de Physique Nucléaire et de Physique des Particules (IN2P3) du Centre National de la Recherche Scientifique (CNRS), établissement Public à caractère Scientifique et Technologique, headquartered at 3 rue Michel Ange, 75794 PARIS Cedex 16, France, – n° SIREN 180 089 013, code APE 7219Z, represented by Mr. Raynald PAIN, acting as head of the ***Direction,*** hereinafter referred to as *IN2P3*,

L'Université de Bordeaux, a scientific, cultural and professional public establishment, having its registered office 35 Place Pey Berlan 33000 Bordeaux, France, represented by its President, Mr. Manuel Tunon De Lara, hereinafter referred to as *UB*,

IN2P3 and *UB* acting in the name and on behalf of *CENBG (UMR 5797)*, managed by Mr Philippe MORETTO, hereinafter collectively referred to as *CENBG*;

Institute of Experimental Physics, Faculty of Physics, University of Warsaw, located at Krakowskie Przedmiescie 26/28, 00-927 Warsaw, Poland; VAT number: PL 5250011266; represented by Vice-Rector for Research and International Relations Prof. Maciej DUSZCZYK, hereinafter referred to as *IEP-UW*.

INTELLECTUAL PROPERTY AND COMMERCIAL USAGE RIGHTS

BACKGROUND

Background means any scientific or technical information, data, samples, design, invention and other technical achievements, patented or non-patented, including but not limited to drawings and formulas, owned or developed by the Parties prior to or independently of this MoU or outside the scope of it and which shall be necessary for the execution of the GES project.

Without prejudice of rights of use granted under this MoU, each Partner shall remain the owner of its Background.

RESULTS

Results means any scientific or technical information, data, samples, design, software, invention and other technical achievements, patentable or not patentable, including but not limited to drawings and formula with all intellectual and industrial property rights whether or not patentable or legally protectable in other forms, resulting from the performance of the GET project under this MoU.

Results shall be promptly identified and reported from one Partner to the other Partners and will be fully disclosed in confidence and the receiving Partner will use its best efforts to prevent their disclosure to third parties.

IP OWNERSHIP

Each Partner will be the exclusive and sole owner of those Results developed by its own personnel under the GES project. Such developments are expected to be the Results of a task assigned to the Partner within the project

and effectively accomplished. Under these conditions the said Partner will be the holder of all the rights including but not limited to intellectual property rights, titles and benefits relating to such Results.

Naturally, this excludes all Background IP developed prior to the GES project and used as a basis for the GES developments; these will remain the property of their respective beneficiaries.

The Results and any intellectual property right jointly developed by the personnel of multiple Partners under the GES project shall be co-owned by such Partners (the ***Co-owners***) proportionally to their respective contributions, whether human, financial or material, to such Results.

Co-owners shall jointly determine which of the Co-owners shall prosecute patent applications for the Result as well as in which countries such patents shall be sought. Co-owners shall cooperate with each other in the prosecution of patent applications resulting from the Results.

Co-owners shall share the expenses incurred in prosecuting patent applications and maintaining patents on the Results in all countries filed by the Co-owners hereto.

If one Partner (Partners) of Co-owners does not desire to file or maintain a patent application on the Results in a country in which the other Partner (Partners) of Co-owners desires to do so, such other Partner (Partners) may keep it thereafter at its sole name and expenses in such country and the non-desiring Partner (Partners) shall give all necessary co-operations for the desiring Partner (Partners) to do so at the desiring Partner's (Partners') expenses. Then, the non-desiring Partner (Partners) shall cease to have any right on such patent application maintained or filed by the desiring Partner (Partners) in such country including but not limited to royalty received from licenses.

EXPLOITATION

Using Rights for GES Partners

Each Partner shall be granted a non-exclusive, non-transferable and free of charge right to use the Results of any other Partner for the following uses, at the exclusion of any other use:

- the performance of the Partner's tasks under the GES project;
- present and future research and studies within the Partner's institution that doesn't involve any use by or any transfer to a third party, and subject to the strict respect of its confidentiality and restrictive use obligations.

In particular, for firmware and software Results, these using rights include full access to source codes.

If such use of Results by a Partner necessitates the use of the Background of another Partner, the using Partner shall be granted a non-exclusive, non-transferable and free of charge right to use the Background for the sole purpose of using Results within the conditions stated above.

Exploitation of own Results

Each Partner is entitled to exploit freely its own Results in any applications field, directly or indirectly through granting of licenses to any third party, and without any financial contribution to be paid to the other GES Partners, within the licensing constraints imposed by the specifics of its development within the GES project (e.g., the commercial or proprietary use of some software developments might be strongly constrained by their use of "contaminating" open-source software license agreements such as the Gnu Public License).

Each Partner may grant licenses for commercial purposes on its Results to the other Partners at their request, subject to third parties rights, on terms and conditions to be mutually agreed by the concerned Partners. Such rights shall be granted under separate written agreements to be concluded between the Partners.

More specifically, as a number of institutes outside the GES collaboration might be interested in purchasing GES hardware, firmware and software modules for their use in scientific projects, the present agreement lays down the principles to be followed for the sharing of the commercial benefits resulting from such purchase. The customer organisations will be referred to as "the Customer".

The different modules developed within the GES project are expected to form an "ecosystem" or "framework" allowing, through proper assembly, the construction and operation of actual systems for specific applications. As such, the modules will often not be usable without being connected to or assembled with or operated by other modules; for instance, a complex electronic board containing an FPGA and a processor needs to be programmed with the proper firmware and software modules to be usable or a front-end board module must include an ASIC module. *When a GES object or subsystem is assembled using multiple GES modules and the IPs of two or more modules are owned by different Partners, all commercial transactions pertaining to each module must be explicitly authorised by all other Partners involved*. *However, all Partners agree to hold this authorisation in abeyance pending to nothing more than reasonable conditions such as the payment of a reasonable fee*.

Exploitation of the joint Results

Each Co-owner shall be entitled to grant licenses on the joint Results to third parties subject to the prior mutual agreement of the other Co-owners regarding thereto and under which royalty, licensed field and other necessary conditions shall be determined.

Any royalty received from licenses on the Results under this subparagraph shall be shared by the Co-owners in accordance with the proportions set forth in section 0.

Use of needed Background

Each Partner is entitled to use Background transmitted by the other Partners which is needed for the exploitation of its Results or the Results of other Partners. Such rights shall be granted under separate written agreements and on terms and conditions to be mutually agreed by the Partners.

Pricing Guidelines

It is recommended that the pricing policy for every product reflects the design, construction and test of the product, in proportion of the actual involvement of the Partner (in terms of engineering hours) for that product. As for the pricing of provided services, it is recommended that it be based on a realistic estimate of the full-time equivalent (FTE) of engineer and/or technician time needed to deliver the service.

Partners' Products and Services Commercial Agreement

For every commercial operation, *every Partner shall produce a specific document stating the pricing policy and licensing specifics for every product that is an instance of a GES hardware, firmware or software module for which the Partner detains IP ownership* (as defined in section 0). *To this end, the Partner will also add the pricing and conditions for all services it intends to provide along with the delivery of said products* (e.g. support, maintenance or training services for the Customer). This document will be referred to as the Commercial Agreement.

Every Partner is expected to provide for the financial and material means for the production, delivery and maintenance of the products it is responsible for, in accordance with the licensing policy it has specified in the

Commercial Agreement. The Commercial Agreement must for instance specify whether the production, testing, maintenance, etc. of a product will be undertaken by the Partner itself, subcontracted to an industrial third party or even carried out by the Customer itself (in which case the Partner receives licensing royalties from the Customer, leaving the responsibility for actual production to the Customer through any means the Customer chooses, provided that all licensing rights and intellectual property are preserved).

Every Partner is also expected to provide for at least the minimal services and full operational documentation needed to install and operate the products coming within the IP ownership of the Partner. The Commercial Agreement shall specify the price and billing procedure for providing these services. As part of these services, *every Partner should provide for a minimal support service through telephone and/or e-mail concerning the products under their responsibility for at least one year*. Typically, any additional support services such as Customer-specific developments or on-site maintenance (involving travel) would have to be negotiated specifically or specified as such.

SCIENTIFIC EXPLOITATION AND ACKNOWLEDGMENT

All scientific and technical publication pertaining to the GES project must be unanimously approved by the project management of every Partner; this approval includes the due citation of all personnel who have substantially contributed to the design and development of the GES modules.

All agreements passed between any Partner and a third party pertaining to the use of GES Results (e.g., the use of GES modules in a physics experiment) shall specify that all publications authored by the third party should include proper acknowledgement of the GES project Results.

CONFIDENTIALITY AND PUBLICATION

CONFIDENTIALITY

Confidential Information shall mean any type of information, patentable, patented or not, notably technical, financial or commercial information, whether oral or written, whatever its form and communication medium may be, notably by samples or models, disclosed directly or indirectly by the disclosing Partner to any other Partner and that the disclosing Partner considers to be its property and of a confidential nature. For the avoidance of doubt, Results and Background of a Partner shall be considered as Confidential Information.

Nothing in the agreement shall affect the ownership of any Confidential Information or any Intellectual Property Rights therein which each Partner makes available to the others under the agreement shall anything herein constitute a license, expressed or implied, from the disclosing Partner to the other Partners to use any of the said Confidential Information or any Intellectual Property Rights therein for any purpose other than the purpose of this MoU.

The Partners undertake to keep strictly confidential and neither to disclose nor to communicate to any third party, by any means whatsoever, any Confidential Information received from the disclosing Partner without the prior written consent of the disclosing Partner, even for the disclosures to new entities, to be potentially part of the GES collaboration.

Notably, none of the Partners shall issue or release any article, advertisement or anything else relating to any Confidential Information or mentioning or implying the name of the other Partners without their prior written consent.

Each receiving Partner shall:

Use at least the same degree of care in protecting Confidential Information against disclosure to any third party as it exercises in protecting its own Confidential Information;

Immediately inform the disclosing Partner in case of loss or theft of any of its Confidential Information.

Each Partner undertakes to disseminate Confidential Information only to its employees who need to have access to it to use it within the scope of the agreement.

Each receiving Partner shall not copy the disclosing Partner's Confidential Information without its prior written consent.

However, the provisions of this section shall not apply to information for which the receiving Partner can prove in writing that:

Such information is or has become publicly known through no wrongful act on its part; or

Such information is available to the public and already known to the receiving Partner at the time of disclosure by the disclosing Partner; or

Such information was rightfully received by the receiving Partner from a third party without breach of the present section or any confidentiality obligation; or

Such information was independently developed or discovered by the receiving Partner without use of a Confidential Information; or

Confidential Information is required to be disclosed to comply with applicable laws or regulations, or with a court or administrative order, provided that the disclosing Partner receives reasonable prior written notice of such disclosure.

PUBLICATION

A Partner intending to make any publication or information communication related to the Project (the ***Publishing Partner***) shall seek written consent from the other Partners. "Written consent" may take the form of e-mail exchanges using institutional e-mail accounts. The Publishing Partner shall furnish the other Partners a copy of such proposed publication or information communication and any other Partner shall within ten (10) days from receipt of the proposed publication or information communication forward their written objections to the Publishing Partner if it determines that its Confidential Information or patentable subject matter may be disclosed and wishes to modify it or to postpone the proposed publication or information communication if needed by real and serious causes. Such postponement shall in no event exceed ninety (90) calendar days from the date of receipt of such objection.

If no written objection is received within the stipulated period of time, the Publishing Partner shall be free to proceed with the publication or information communication. Each information communication or publication shall reference to the cooperation of all the Partners.

FUNDING

The funds available through the ENSAR-2, EU project will cover the expenses associated with some of the development defined in ANNEX 2. With unanimous agreement between all partners, this funding section can be modified at a later stage. Given the limited funds available in the GES project, it is understood that additional funds be sought by the Partners to allow necessary expenditures to be undertaken.

The budget for the GES programme is covered **in part** by the ENSAR2 TecHIBA/GES of a total of 50 k€. Given the relatively small ENSAR2 budget, the individual labs will cover the remaining different needs of the project. The ENSAR2 budget will be distributed by Irfu to the individual labs, in conformity with EU regulations.

The GES programme will cover the submission of the FPCSA ASIC and the PCB manufacture that goes with it. Namely what is termed as CHIP CARDS. GES will also cover the purchase of FPGA cards that will be integrated onto the PCB to make up the hardware for the tasks noted as in the table below.

The table includes a modest amount of travel expenses for meetings and exchanges. ENSAR2/GES will not cover any human resources. The budget for human resources will be provided by the Partners. The travel funds (*) will not be issued from ENSAR2 programme but raised from other resources.

The ENSAR2/GES will not cover any production of the hardware that is to be valorised through appropriate channels. However, the engaged resources will endeavour to produce prototypes that can be reproduced industrially to this end. It is at the discretion of the individual labs to reinject part or all of the valorisation into the project.

Institute	Irfu	CENBG	UoW
ASIC Submission	17 000 €	0 €	0 €
PCB	0 €	9 000 €	8 000 €
Travel	6 000 €	0 000 €*	000 €*
FPGA Cards	0 €	4 000 €	6 000 €
TOTAL	23 000 €	13 000 €	14 000 €

SCHEDULE

The GES project is programmed to be completed in 36 months beginning January 2017. A schedule with named persons in charge for the completion of the different tasks will be set along with the provisions in cases where engineering time is no longer available. The schedule can be modified at later stages by unanimous agreement between Partners.

GOVERNANCE

STEERING COMMITTEE

The GES project will be coordinated by a *steering committee* comprising *one* representative per Partner, with decision power pertaining to policy, funding and spending. All executive decisions must be validated by a unanimous agreement between representatives. Every representative can be assisted by any number of experts in all meetings and discussions. Every representative can delegate some or all of their decision prerogatives to

another person. Such delegations must be explicitly notified to the steering committee in written form (e.g., e-mail) before every official meeting or discussion of the steering committee. The names of the representatives for every Partner institute are given below. Every Partner institute can assign another representative to the steering committee provided that the steering committee is duly notified in written form.

NAMES OF THE STEERING COMMITTEE REPRESENTATIVES

- *CEA Irfu*: Mr. Éric DELAGNES, eric.delagnes@cea.fr, +33 1 69 08 22 52

- *IEP-UW*: Prof. Wojciech DOMINIK, Wojtek.Dominik@fuw.edu.pl, +48 22 55 32 806

- *CENBG*: Mr. Jean-Louis PEDROZA, pedroza@cenbg.in2p3.fr, +33 5 57 12 08 29

Appendix 2: Work Packages

Collaboration and Goals

Following the widespread use of the GET electronics and software system by more than 20 laboratories throughout the world, a number of performance and technical needs have arisen, which call for further developments. At the same time, considering the widespread limitation of financial and human resources in most institutes, it appears that modular designs and generic approaches must be encouraged in order to maximise reuse of software (SW), firmware (FW) and hardware (HW) developments.

A number of informal discussions involving Irfu, CENBG and Warsaw University (WU) have taken place, allowing to establish the different needs and a collaborative scheme where different parts of a modular design can be regrouped as work packages (WP) and distributed among the collaborating institutes. This document is an attempt at such a description regrouped under the GES (Generic Electronics for Systems) acronym.

The GANIL institute has also expressed interest in GES and is expected—in a first stage—to assign one or more engineers as observers. Eventually, an actual contribution to the evolution of the GET µTCA electronics along the GES concepts is considered. In the same way, Leuven University considers contributing to the project through the development of GPU-based algorithm for the fast analysis of acquisition data.

As GES is part of the TecHIBA programme, the GES results and achievements will be presented to the annual TecHIBA meetings.

A concrete goal of the project will be to deliver demonstrator modules (see further) that will include at least all the hardware, firmware and software parts defined as the basic bricks of the GES generic architecture. The modules will have to be functional and sufficiently documented for all interested parties to be able to continue the work.

Genericity

The concept of “genericity” is central throughout this document so that we need to define it as precisely as possible in order to steer the different engineering activities towards a coherent common goal. A *generic* system as we envisage it here, is a system that boasts the following features:

- it is *modular*, meaning that all the software, firmware and hardware are divided into *modules*, i.e. parts that tackle a very limited aspect or functionality of the system and can be connected to other parts through a simple and limited interface;
- the functionality or aspect attached to a module are obtained by abstracting out typical issues, parameters and concepts pertaining to a class of entities or objects at hand;

- all modules can be *configured* by using a set of parameters which are relevant to the functionality of the module and which can cover a "wide enough" variability space;
- module interfaces include precise definition of *protocols* that must be followed by all modules designed with the goal of being integrated in the system; it is expected that protocols can themselves be configured through a set of relevant parameters.

NEEDS

TARGET SYSTEMS

1. Generic, versatile electronic platform implementing multiple components needed to test new ASICs.
2. Acquisition electronics for small or prototype AGET-based physics projects.
3. Acquisition electronics for mid-size AGET-based projects that need multiple, synchronised boards.
4. Acquisition electronics for small or prototype projects using other ASICs, including educational tools.
5. Electronics for single clock distribution, trigger synchronisation and basic trigger schemes.
6. µTCA-based acquisition electronics for larger experiments.

CONSTRAINTS

1. Maximise reuse through modular design for HW, FW and SW; also allows distribution of work.
2. Maximise compatibility with GET HW, FW or SW modules to allow for modular upgrades.
3. Follow "component-oriented" design for HW, FW and SW: boxes implementing well-defined interface.
4. Aim at "turnkey" packages, easy to download, install and learn; support multiple platforms; in particular, develop firmware as IPs wherever possible and software as framework/libraries/plugins.

ARCHITECTURE PRINCIPLES

GENERIC PLATFORM FOR TESTING NEW ASICS

Target 1 in the "Target systems" list above is arguably the most extended setup in the sense that it needs the greatest number of HW component types and their associated FH and SW. It can be summarised in Figure 2. ***The Digital Backend itself is expected to be divided into a COTS module and a "motherboard" featuring all additional connectors and components***. This system allows ASIC designers to rapidly design a simple PCB with a single ASIC so as to test the ASIC using a "standardised" reusable electronic platform. Such a design is clearly not adapted to actual experiments for multiple reasons, e.g. the connector between ASIC and ADC.

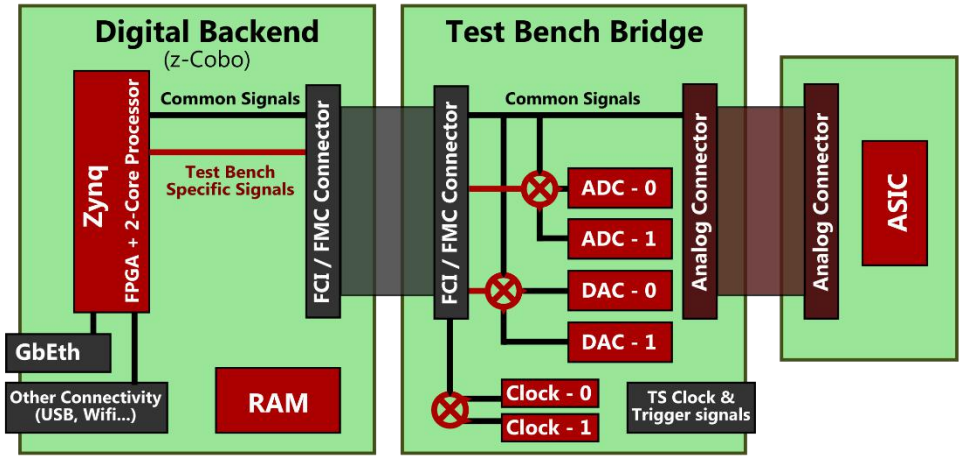


Figure 2: Test bench hardware setup.

However, the different FW and SW modules, also possibly some HW schematics can be reused for the design of an application-oriented board regrouping one or more ASIC chips with their single choice of ADC, DAC and other components. It is important that the designs are made having in mind future reuse in other target applications (targets 2 to 6).

Clock Distribution and Common Trigger

Systems that use multiple acquisition boards usually need to share a common clock, a common time-stamp reset signal and a common trigger signal. The GES project needs at least a basic version of such a card in order to test multi-board configurations. An improved version of the card designed for the Minos experiment at Irfu is expected to be built for other projects. This card (let's call it TCM-G) can be designed from the outset with a GES-compatible interface.

Main Firmware and Software Component

The main FW and SW components are represented in Figure 1, where triple arrows represent acquisition data

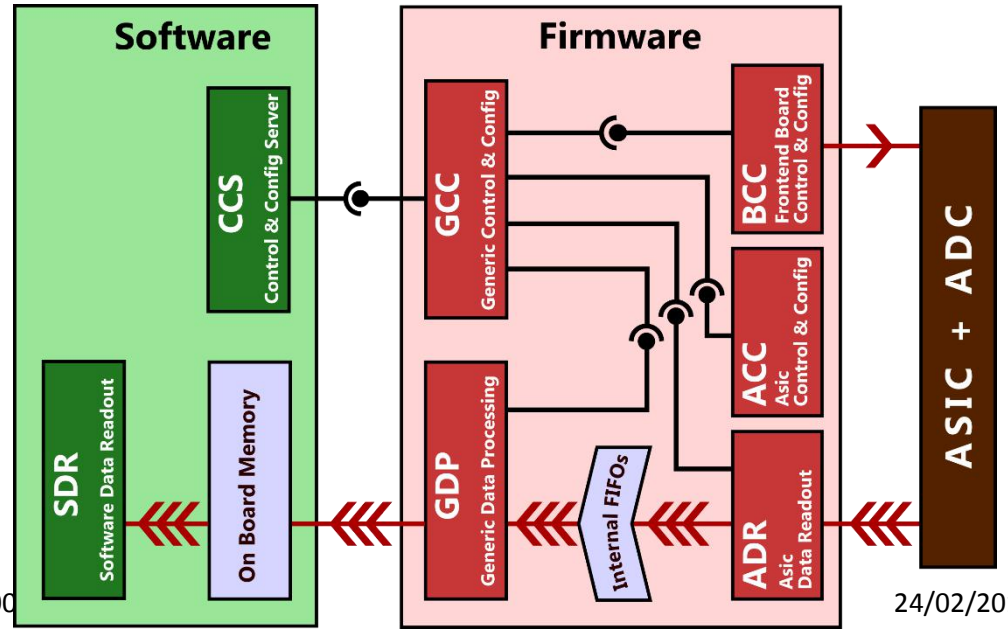


Figure 1: Main firmware & software components.

flows and handle connectors represent the connection between a “client” module and the interface of the a “server” module. The following table gives a brief description of the functionalities implemented by these modules:

FIRMWARE	Front-end ASIC control & configuration FW, implementing all interactions with ASIC that allow it to be configured and controlled.	ACC
	Front-end board control & configuration FW, implementing all specifics of interactions with front-end board components other than ASICs (includes power supply control, HW monitoring…).	BCC
	Front-end ASIC data readout FW, implementing all interactions with ASIC for data readout.	ADR
	Back-end control & configuration FW, implementing the sequences of a generic memory mapped protocol the configuration and control of the different modules; this module represents the different state machines controlling the acquisition process and is stimulated by the CCS SW module. Also includes the FW for trigger logic and time stamping.	GCC
	Downstream data processing FW, implementing at least the transfer of data into memory over the network. It can also apply some processing of the data “on the fly”.	GDP
SOFTWARE	Control and configuration software server, implementing all interactions with the GCC and the GDP (kind of “driver”).	CCS
	Software data readout, implementing all interactions with GDP usually using circular buffers as intermediate storage. This module is not needed if the FDP directly sends its data over the network (e.g., direct firmware TCP/UDP).	SDR

SOME TECHNOLOGICAL CHOICES

Numerous different needs have been discussed by the parties. All parties involved in the discussion favour solutions based on the Xilinx Zynq SoC solution for the digital backend COTS module. In view of price constraints, the ZedBoard family of modules and boards seem well adapted for a Zynq-based system. I/O capabilities (number of pins), network performance capabilities (possibilities for fibre optics and multi-gigabit transmission) and small form factor seem to favour the PicoZed module[1] although it lacks the possibility to run standalone (no standalone power supply or Ethernet connector): this means that the board bearing the module must implement the desired network connectors and power supply capabilities. Also, contrary to the ZedBoard, the PicoZed features FCI connectors instead of FMC. This choice needs to be further discussed.

[1] See website http://zedboard.org/product/picozed.

WORK PACKAGES AND RESPONSIBILITIES

In view of the brief architecture and modules description, here is a tentative work package list and their associated labs responsible for their development:

1) Generic CCS and SDR Software modules ..... Irfu & CENBG
   All hardware and firmware modules are expected to be operated by these same software modules.
2) Generic GDP and GCC Firmware modules ..... Irfu & UW
   All hardware and firmware modules are expected to be operated by these same software modules. Detailed specifications must be established before the FW is actually developed.
3) Downstream DAQ Software ..... Irfu
4) Test Bench Bridge (TBB) for a generic ASIC test bench: a set of boards to test various ASICs with a choice of ADC, DAC, etc. components.
   a. HW – TBB board ..... Irfu
   b. FW – BCC, ADR and ACC for different ADC and ASICs ..... Irfu
5) z-CoBo: a Zynq-based reduced CoBo board replacing the obsolete ML507 from Xilinx operating a GET AsAd card. This module benefits from the ENSAR2 project funds.
   a. HW – Commercial Card (e.g. PicoZed) Base board ..... UW
   b. FW – AsAd-BCC, AsAd-ACC, AsAd-ADR ..... UW
   c. SW – Compatibility with GET Software ..... Irfu
6) SAM (**S**ingle **A**get **M**odule): for small experiments (less than 256 channels), a single AGET together with its ADC and pulser, controlled by a Zynq SoC. A first version of this board has already been developed by CENBG together with minimal FW and SW allowing it be readily used with the GET test bench software (GetController).
   a. HW – Board ..... CENBG
   b. FW – SAM-BCC, SAM-ACC, SAM-ADR ..... CENBG
   c. SW – Compatibility with GET Software ..... Irfu & CENBG
7) TEC **T**ime & Energy **C**ard: a frontend with ATHED ASICs[2] with track and hold and time-to-amplitude conversion.
   a. HW – Board ..... CENBG
   b. FW: TEC-BCC, TEC-ACC, TEC-ADR ..... CENBG
8) CC (**C**hip Carrier) **C**ard: a card with FPCSA ASICs for a large dynamic and large resolution very frontend.[3] This module benefits from the ENSAR2 project developments.
   a. HW – FPCSA ..... Irfu

[2] ATHED was developed by Irfu/Sédi for the Must-II programme - 16 channels yielding multiplexed analogue step function for energy and time.

[3] Multi-channel external PAC on AGET yielding an extended dynamic range for gas and solid-state counters.

b. HW – Chip Card ..... CENBG
c. FW – CC-BCC, CC-ACC, CC-ADR ..... CENBG

9) TDCM-G: Clock distribution and common trigger board derived from the Minos TCM card for PandaX-III; adapt to use with GES system.
   a. HW – TDCM-G Board..... Irfu
   b. FW – Specific ..... Irfu
   c. SW – Integration with GES Software..... Irfu

GENERIC IPS

IPs are common subsystem parts which can be freely used by all the partners of a yet-to-be-defined Memorandum of Understanding (MoU). An IP can be materialised by hardware or firmware or software. The MoU must clearly specify the responsibilities of each partner in term of property, purpose of the IPs in a development and impact of possible valorisation. Generics IPs are therefore pieces of a system that can be integrated in various modules for various projects. The 5 work packages described are expected to use these generic IPs. The working concept covered by the term "generic" is the flagship of the GES project.

ENSAR2 PROJECT SPECIFICS

CC card: The FPCAS ASICs (designed by Irfu) will be implemented on a “SuperZap” board to be connected to a standard GET system. Such a configuration needs to host a local digital environment for slow control through an extra communication channel for monitoring and pulse generator. An alternative way is to design a board populated with a Zynq FPGA. A 2x2 FCSA ASIC with differential output prototype board has been designed and tested at Irfu. In a first phase CENBG will test this prototype to check the behaviour and performances with a differential to asymmetric analogue output. A new FPCSA ASIC will be designed by Irfu to increase the number of channels (16 or 32), introduce a slow control to include different gains and levels of switching from one gain to another and introduce a saturation protection analogue circuit. A new form factor (QFN40, 6x6 mm, pitch 0.5 mm) will be adopted. The prototype board is expected to be designed by CENBG. The CC card is of interest for many physicists involved in experiments with Si and gas media where light and heavy ions are to be detected.

z-CoBo: Warsaw University has developed an FMC-to-VHDCI adapter card allowing to connect a ZedBoard to a GET AsAd board. The FW must be either developed from scratch or adapted from the GET MSU FW.

Generic ASIC test bench platform: The goal of this platform is to provide tools allowing rapid test bench deployment for testing future Irfu ASICs. The need is that of a generic backend that holds everything needed to test a new ASIC design, including pulse generators, DACs, ADCs… so that the ASIC is soldered on a small card with no other complex components. Such a generic backend looks very much like the typical “simple experiment” backend with additional components used to send stimuli to the ASIC. In order to maximise reusability, we should dissociate this platform in 2 boards: one being the generic digital backend for control and configuration of the ASIC and readout of digitised data (Digital Backend based on PicoZed module or other), and the other featuring all the additional hardware components needed to stimulate the ASIC and run tests in precisely controlled contexts

(Test Bench Bridge). From the firmware point of view 5 reusable IPs are identified: ACC (Asic Control & Config), ADR (Asic data Readout), GDP (Generic Data Processing), GCC (Generic Control & Config) and TL (Trigger Logic). On the software side 2 main block are identified: SDR (Software Data readout) and CCS (Control & Config Server). IPs can be inserted in all the modules described above.

Appendix 3: GES FPCSA specifications

In order to fulfil the demanding requirements in terms of dynamic range and at the same time to ensure a high genericity, we propose to design a new multi-channel ASIC based on a floating-point Charge Sensitive Amplifier **FPCSA** architecture. This architecture is based on automatic gain switching during the rise time of the pulse. By default, the **CSA** is configured in a high gain mode. If the charge exceeds a specific value, the CSA automatically switches to a low gain value. Thanks to this basic principle, one can reach high dynamic range and high energy resolution.

MAIN REQUIREMENTS

The main requirements that we propose for this new **GES FPCSA ASIC** are listed below:

- Multi-channel ASIC: 16 or 32. The final number of channel will be driven by the power consumption per channel.
- Technology: we intend to use the same technology as the one used for AGET and FPCSA ASICs. The GES-FPCSA will be designed in the AMS CMOS 0.35 µm.
- SPI serial interface. We intend to integrate an SPI communication protocol. The Slow-Control of the new ASIC will be based on a SPI-like protocol that has already been used in many of our ASICs like the AGET family and the IDeF-X family (ref-1) for instance. It will be based on a 4-signal protocol: DATAIN DATAOUT SlowControl and STROBE.
- Digital output signal format: depending on the number of PAD in the new ASIC, the possibility of implementing CMOS to LVDS and LVDS to CMOS drivers in the ASIC will be considered.
- Bi-directional. In order to be able to read both types of electrode (anode and cathode of DSSD for instance) the ASIC must be able to deal with both polarities of input signal.
- Coupling to detector: the baseline is to be AC coupled to detector. The ASIC will not be designed to “feed” the detector in current.
- Temperature range: -40-+40: since the ASIC could be used to read silicon semi-conductor detectors that are generally cooled down for noise reduction purpose, the chip must remain operational from -40 to +40 °C.
- Low threshold: The minimal detectable energy is set to 200-300KeV for Silicon, as for the FPCSA.
- Saturation. The saturation is a critical problem, especially in multi-channel ASICs: when one specific channel saturates, the neighbouring channels can be considerably impacted. The consequence is generally that even if only one channel saturates, the whole ASIC is blind for a duration that depends on the charge and of the fundamentals time constant of the CSA. We proposed to try to integrate an anti-saturation circuit. This could be made by a smart feedback circuit coupled to the CSA.

- 2 Gains adjustable by Slow Control:
  - High 1 pC to 4pC
  - Low 7pC to 42pC (1GeV silicon)
- Output signal: in order to be compatible with the output of the AGET ASIC, the output analogue signals will be single-ended with AGET-compliant baseline and dynamic range.
- Dead time. The fall time of the CSA will contribute to the whole dead time of the system using GES-FPCSA. We intend to make this time configurable by slow control. The range could typically be set between few hundreds of nano-seconds and few micro-seconds.

Ref:

Ref. 1-Gevin, O., Lemaire, O., Lugiez, F., Michalowska, A, Baron, P., Limousin, O., & Delagnes, E. (2012). Imaging X-ray detector front-end with high dynamic range: IDeF-X HD. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, A 695 (2012) 415-419.

PROPOSED ARCHITECTURE

The FPCSA architecture is presented on **Erreur ! Source du renvoi introuvable.**.

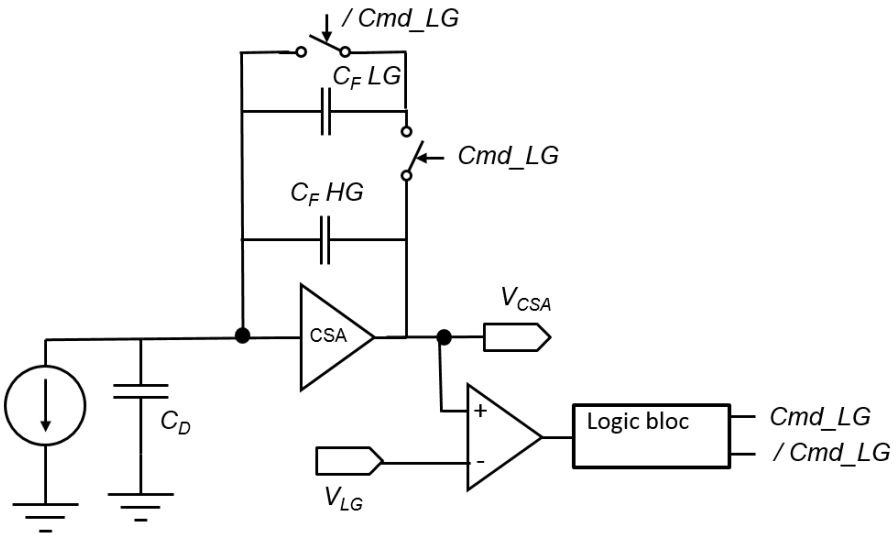


Figure 3 : architecture of the FPCSA V2

In the low energy range, typically between 100 keV and 15 MeV, the CSA works in its high gain mode. The charge is integrated in C_F *HG* small feedback capacity of about 500 fF. Figure 4 shows the FPCSA output for low energy events (left) and for high energy events (right).

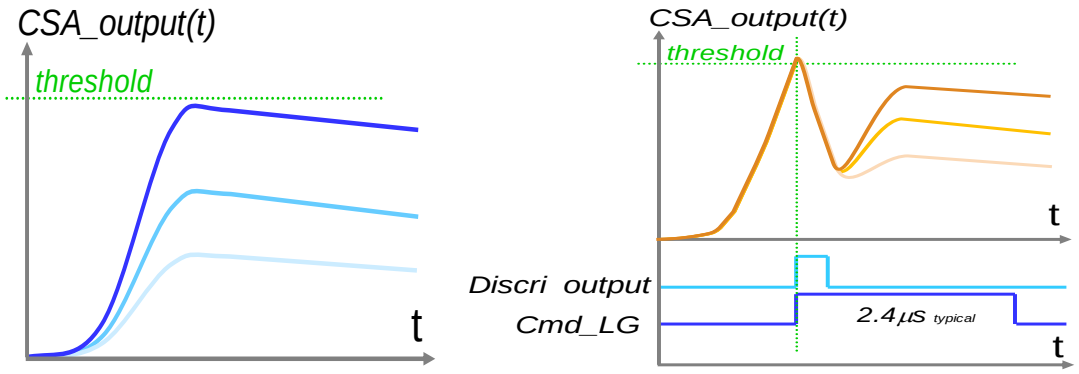


Figure 4 : CSA output for low energy events (left) and for high energy events (right)

When the output signal reaches a high-level threshold V_{LG}, a low gain capacitor C_F *LG* is added in parallel to the other. Consequently, the gain of the CSA decreases and the output signal returns to the baseline quickly in few nano-seconds and settles to its final value in about 30 ns. In addition, a dedicated output signal called “cmd LG” indicates if a low gain event was detected. The automatic configuration controller is operated by a command bloc composes by a comparator and a monostable.

The global architecture of the multi-channel GES-FPCSA chip is presented in Figure 5.

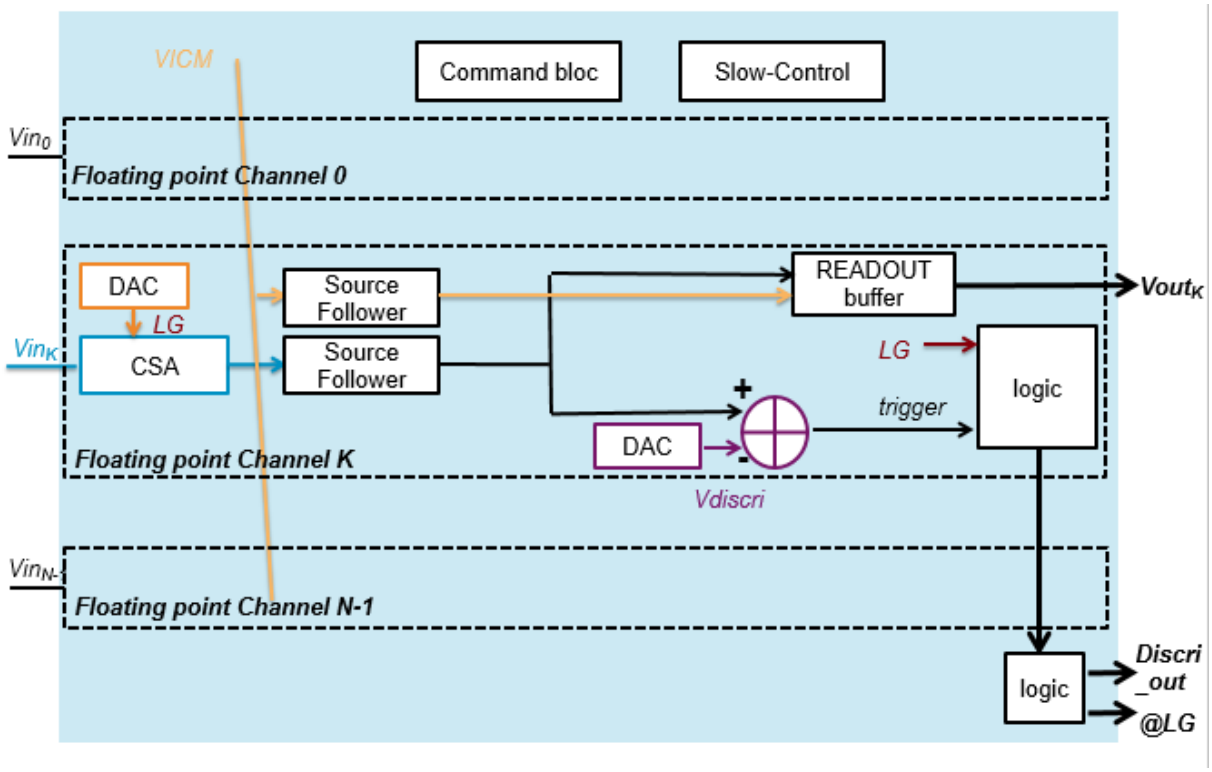
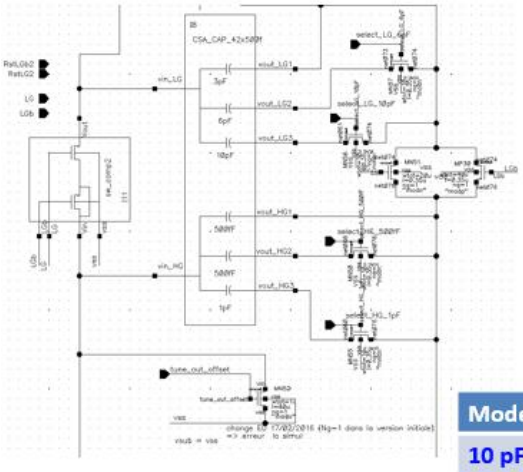


Figure 5 : global architecture of the multi-channel FPCSA V2 chip

A channel is built of the double gain CSA with a LG discriminator programmable with a DAC. A source follower is placed at the output of the CSA to readout this output. Another discriminator is used to detect if an event exceeds the threshold Vdiscr. A DAC is added to programme the threshold of this detection.

The slow-control block is common of all the chip SPI link.

2 gains considered and are programmable by Slow Control:



HighGain : C_f = 500 fF
Select adding : 500 fF
Select adding : 1 pF

Low Gain : C_f = 3pF
Select adding : 6 pF
Select adding : 10 pF

Mode	SEL_HG	SEL_LG
10 pF	0	0
10 pF + 6 pF	0	1
10 pF + 500 fF	1	0
10 pF + 6 pF + 500 fF	1	1

FIRST SIMULATIONS

Figure 6 presents the transient output signal of the CSA for different energies [1 – 600 MeV] with Cd = 200 pF, V_Trigger = 1,31 V and V_LG = 2,3 V

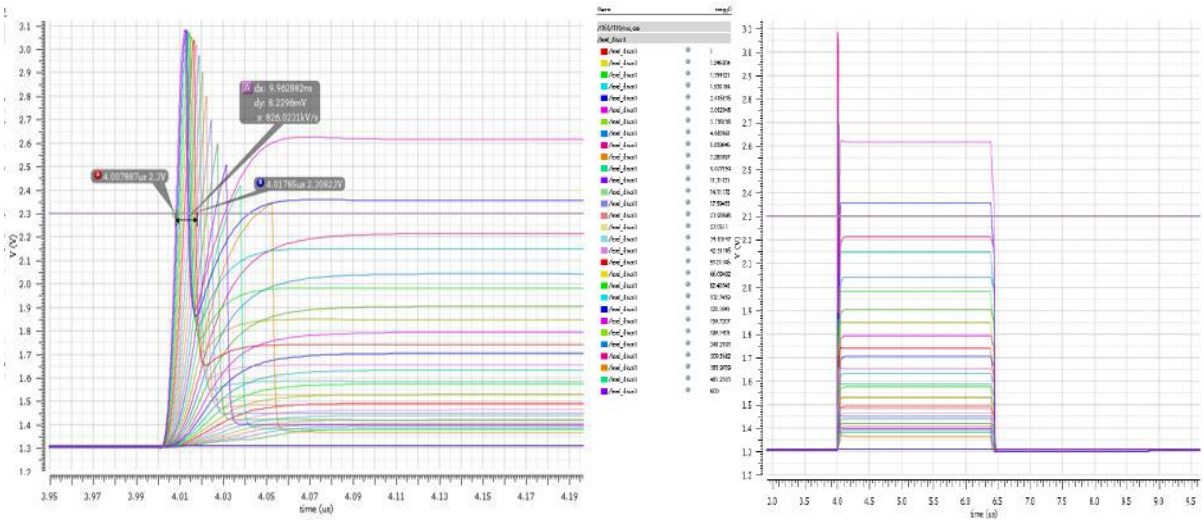


Figure 6 : Transient output signal of the CSA for different energies [1 – 600 MeV] with Cd = 200 pF, V_Trigger = 1,31 V and V_LG = 2,3 V

The triggering of the FPCSA is quite fast (around 30 ns) and the dead time is lower than 150 ns.

Figure 7 presents the linearity of the CSA for different energies [1 – 600 MeV] Cd = 200 pF, V_Trigger = 1,31 V and V_LG = 2,3 V

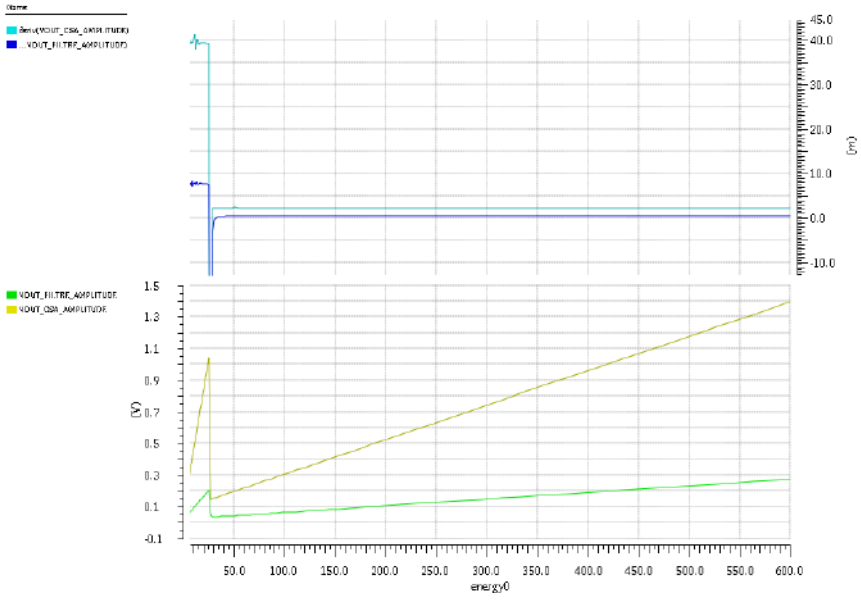


Figure 7 : the linearity of the CSA for different energies [1 – 600 MeV] Cd = 200 pF, V_Trigger = 1,31 V and V_LG = 2,3 V

- High gain: 1 MeV to 25 MeV.

- Low gain: 25 MeV to 500 MeV.

Transient noise analysis permits to have a good estimation of the noise of the CSA. For that, we used a perfect filter at the CSA output to evaluate the noise generate by the CSA.

Figure 8 shows the transient noise analysis of the **High GAIN with** 100 runs, Noise Fmax = 10 MHz, Fmin = 100, Noise seed = 1 and noise scale = 100 with Cd = 60 pF, input MOS 8 mm

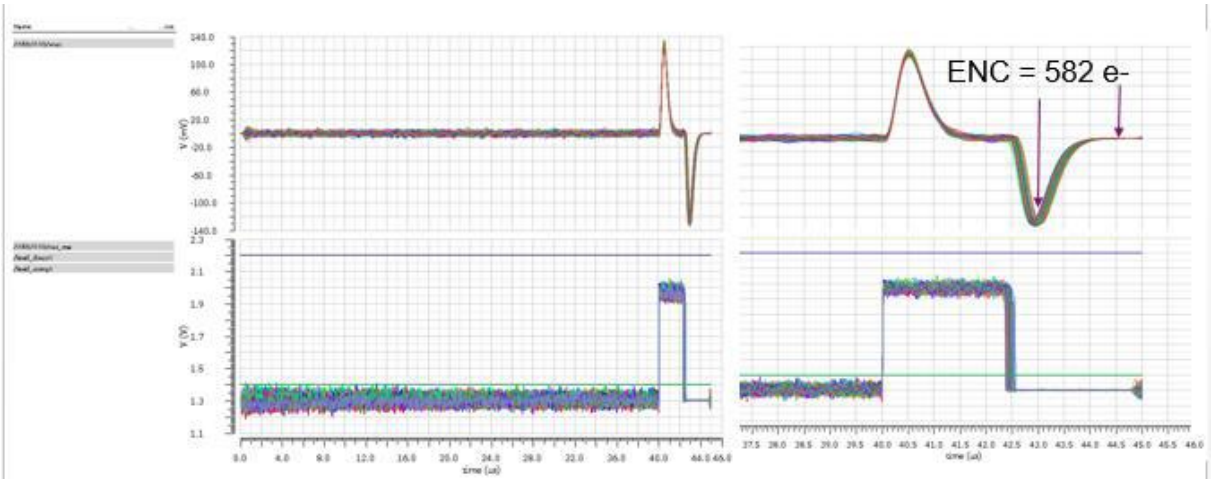


Figure 8 : transient noise analysis of the High GAIN with 100 runs, Noise Fmax = 10 MHz, Fmin = 100, Noise seed = 1 and noise scale = 100 with Cd = 60 pF, input MOS 8 mm

The equivalent noise charge (ENC) is expressed:

ENC = (((stddev((value(VT("filter at the CSA output ") 4.5e-05) - ymin(VT("filter at the CSA output "))))) / average((value(VT("filter at the CSA output ") 4.5e-05) - ymin(VT("filter at the CSA output "))))) * VAR("energy0") * 1000000.0) / 3.6 / 100)

The ENC simulates for high gain is 582 e-

Figure 9shows the transient noise analysis of the **low GAIN with** 100 runs, Noise Fmax = 10 MHz, Fmin = 100, Noise seed = 1 and noise scale = 100 with Cd = 60 pF, input MOS 8 mm

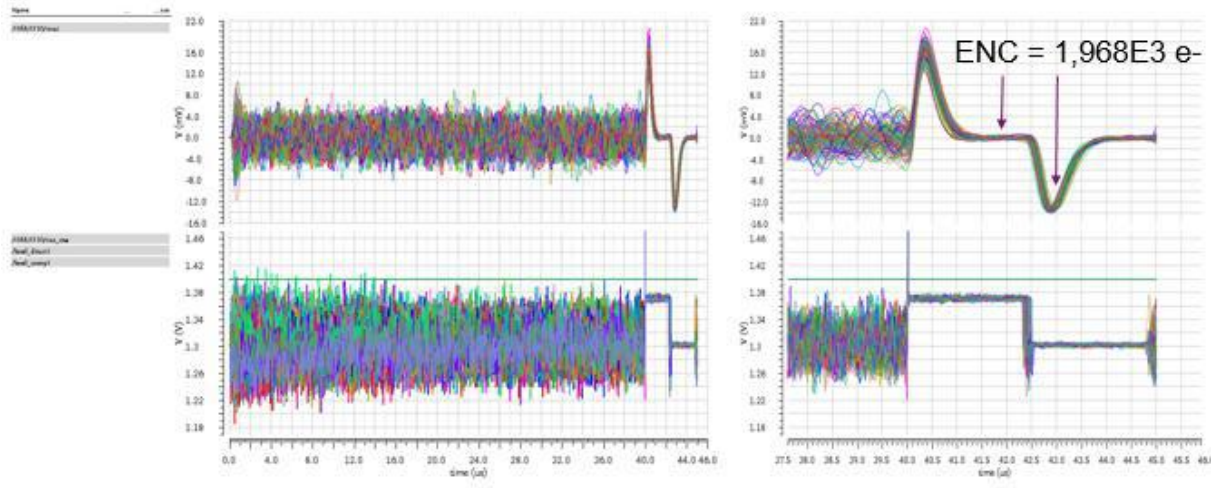


Figure 9 : transient noise analysis of the Low GAIN with 100 runs, Noise Fmax = 10 MHz, Fmin = 100, Noise seed = 1 and noise scale = 100 with Cd = 60 pF, input MOS 8 mm

The ENC simulates for low gain is 1968 e-